Interfacial Oxide Layer Scavenging in Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$-Based MOS Structures With Ge Channel for Reduced Write Voltages

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***Abstract*— Strategies to reduce the interfacial oxide layer thickness in ferroelectric (FE) $Hf_{0.5}Zr_{0.5}O_2$ (HZO) metal-oxide-semiconductor capacitor (FE-MOS) structures on Ge and Si substrates were investigated by electrode engineering, as means to reduce the write voltage in FE field-effect transistors (FEFETs). When the gate metal in Ge FE-MOS capacitors is changed from W (control) to Pt/Ti, the coercive voltage is reduced from ∼2.5 to ∼0.9 V (a 66% reduction) along with a 64% increase in the capacitance consistent with an interfacial layer (IL) thinning. High-resolution scanning transmission electron microscopy (HR-STEM) reveals no visible IL with Pt/Ti electrodes in Ge FE-MOS, suggesting the scavenging of oxygen from the GeO_x IL by the Pt/Ti electrode. However, a much smaller reduction of the coercive voltage was observed on Si FE-MOS structures with Pt/Ti electrodes. In this study, it is demonstrated that IL thinning might provide a pathway to reduce the write voltage in FEFETs based on conventional semiconductor channel materials down to a logic-compatible level.**

***Index Terms*— FE metal-insulator-metal (MIM) capacitor, ferroelectric (FE) metal-oxide-semiconductor (MOS) capacitor, Ge, $Hf_{0.5}Zr_{0.5}O_2$ (HZO), oxygen-scavenging, write voltage.**

I. Introduction

FERROELECTRIC field effect transistors (FEFETs) are a promising candidate for embedded non-volatile memory applications [1], [2], [3], [4]. To improve device performance, write voltages below 1.5 V are required [2]. In a Si-channel FEFET, most of the gate voltage drop is across the low-κ SiO_2 interfacial layer (IL). Only a small fraction of the voltage is across the ferroelectric (FE) film. This drives the write voltage beyond 2.5 V. To reduce FEFET write voltage, increasing the κ-value of the IL or reducing its thickness are potential strategies [5], [6], [7], [8], [9], [10]. Ge has been reported as a good alternative channel material [11], [12]. Ge channel FEFETs show a lower write voltage than Si channel FEFETs due to the thinner and higher κ-value interfacial GeO_x layer [13]. In addition, the GeO_2 layer has lower thermal stability than SiO_2 making it easy to getter by a reactive metal electrode such as Ti [14]. In the gettering process, oxygen is removed from the IL (GeO_x or SiO_2) to form TiO_x at the top of the gate-stack thereby reducing the thickness of the IL [15].

In this study, IL thinning strategies are reported for FE-MOS structures on Ge and Si substrates with $Hf_{0.5}Zr_{0.5}O_2$ (HZO) as the FE layer. Electrical characterization techniques (capacitance-voltage, polarization-voltage hysteresis loop, and positive-up-negative-down, PUND measurements) and high-resolution scanning transmission electron microscopy (HR-STEM) were performed to study the impact of IL gettering on write voltage of HZO-Ge FE-MOS structure. Three different electrode combinations (Pt/Ti/TiN, Pt/Ti, and W) were employed to study the effect of oxygen scavenging on the IL. To decouple the impact of the electrodes on the IL and

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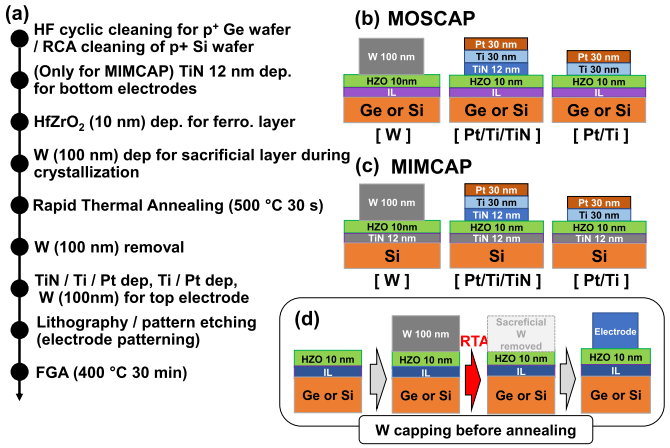

Fig. 1. Process Flow and Device Structures. (a) Process flow. (b) Device structures of the fabricated HZO MOS capacitor. (c) Device structures of HZO MIM capacitor. (d) W capping scheme. For each Ge and Si substrate, three different devices (W, Pt/Ti/TiN, and Pt/Ti) were fabricated for comparison. W capping scheme was used to minimize the influence of top electrodes during the RTA process.

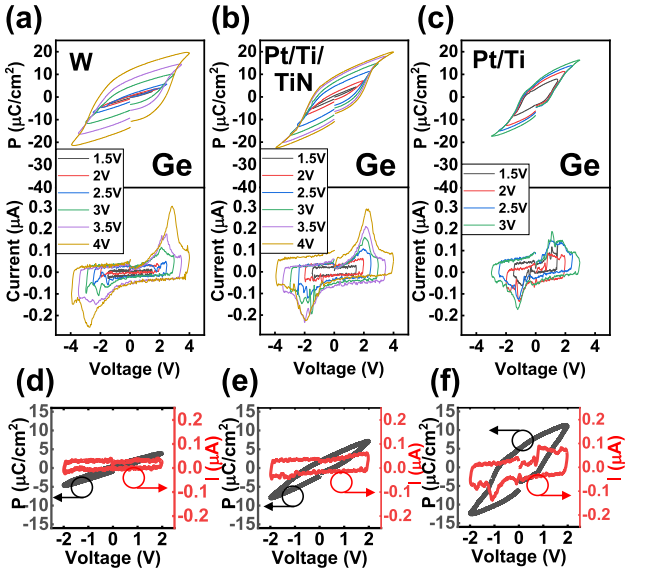

Fig. 2. *P*–*V* and *I*–*V* Measurements for three electrode structures on Ge substrates. (a) W electrode with Ge substrate at various voltage sweep ranges. (b) Pt/Ti/TiN electrode with Ge substrate. (c) Pt/Ti electrode with Ge substrate. (d)–(f) *P*–*V*/*I*–*V* measurements for W, Pt/Ti/TiN, and Pt/Ti electrodes at a smaller voltage sweep range.

the FE layer, FE metal-insulator-metal (MIM) structures were studied with the same set of electrodes. The IL scavenging using Pt/Ti gate electrode can lead to a dramatic 66% reduction of the V_c in Ge FE-MOS capacitors compared to W-gated capacitors which do not show IL scavenging. However, the same IL thinning strategies are not as effective on Si substrates consistent with the higher thermodynamic stability of SiO_2 compared to GeO_2.

II. Experimental Details

Fig. 1(a) shows the fabrication process flow for the $Hf_{0.5}Zr_{0.5}O_2$ (HZO)-based metal-oxide-semiconductor (MOS) capacitors with Ge (Ga-doped p^+, 0.05 $\Omega \cdot$ cm) and Si (B-doped p^+, 0.05 $\Omega \cdot$cm) substrates. Before HZO deposition, cyclic pretreatments (3 × HF rinse) for Ge and RCA cleaning for Si were performed. 12 nm TiN bottom electrodes for MIM device structures [Fig. 1(c)] were deposited by atomic layer deposition (ALD) using a Veeco Fiji G2 ALD system. A 10 nm HZO layer was deposited by thermal ALD at 250 °C in Ar purge in the same ALD system without vacuum break. Tetrakis(dimethylamino)hafnium (TDMAH), tetrakis(dimethylamino)zirconium (TDMAZ), and H_2O precursors were used for the HZO ALD process [16], [17]. To minimize the capping effect during crystallization, a sacrificial W layer was deposited followed by a rapid thermal annealing (RTA) step at 500 °C for 30 s to crystallize the HZO film. After the crystallization process, the W layer was removed by hexafluoride (SF_6) and O_2 reactive ion etch (RIE) [Fig. 1(d)]. Thereafter, three different electrodes were deposited: Pt/Ti/TiN (30/30/12 nm), Pt/Ti (30/30 nm), and W (100 nm). A Denton e-beam evaporator and a Unifilm sputterer were used for Pt/Ti and W deposition, respectively. After electrode patterning, a forming gas anneal was performed at 400 °C for 30 min to induce the gettering process.

Electrical measurements were conducted using an aixACCT TF 3000 analyzer and a Keysight B1500A semiconductor device analyzer. The polarization–voltage (*P*–*V*) measurements and the PUND measurements were conducted at a frequency of 1 kHz with aixACCT TF 3000 analyzer. The dynamic leakage-current-compensation (DLCC) scheme was applied to the *P*–*V* measurements [18]. Capacitance (*C*)–voltage characteristics were measured at 100 kHz using a Keysight E4990A impedance analyzer.

III. Results and Discussion

The polarization–voltage (*P*–*V*) and switching current-voltage (I_{sw}–*V*) characteristics of Ge MOS capacitors are shown in Fig. 2. The *P*–*V* and *I*–*V* minor loop characteristics for the three different top electrodes with the voltage sweep ranges are shown in Fig. 2(a)–(c). The maximum voltage sweep range for a given FE-MOS capacitor was chosen to be the maximum voltage that could be safely applied without causing an electrical breakdown of the oxide film. Fig. 2(d)–(f) displays *P*–*V* and *I*–*V* characteristics for a smaller voltage range (−2 to 2 V) with the three electrodes. Fig. 2(d)–(f) confirms that only the Pt/Ti samples exhibit a hysteresis loop due to FE switching in the voltage range −2 to 2 V indicating that the Pt/Ti device has the lowest V_c.

Fig. 3 shows the *P*–*V* and *I*–*V* characteristics of FE MOS capacitors on Si. Fig. 3(a)–(c) depicts the minor loops of the *P*–*V* and *I*–*V* characteristics for the three electrodes at various voltage sweep ranges. Fig. 3(d)–(f) displays the *P*–*V* and *I*–*V* characteristics in a smaller voltage sweep range of −3.5 to 3.5 V with various electrodes. In Fig. 3(d)–(f), it can be seen that only the Pt/Ti samples have a hysteresis loop caused by FE switching in the voltage range of −3.5 to 3.5 V. This trend is similar to Ge, and it indicates that the capacitors with Pt/Ti electrodes have the lowest V_c.

Fig. 4(a)–(c) shows the minor loops of the *P*–*V* and *I*–*V* characteristics in the FE MIM capacitor with the three different

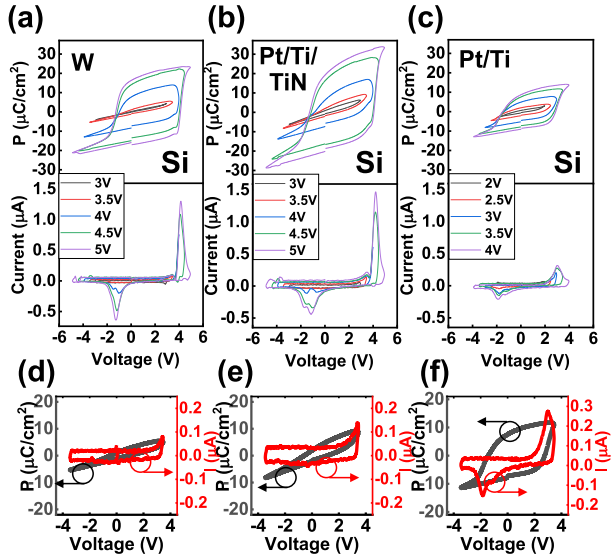

Fig. 3. *P–V* and *I–V* measurements for three electrode structures on Si substrates. (a) W electrode with Si substrate at various voltage sweep ranges. (b) Pt/Ti/TiN electrode with Si substrate. (c) Pt/Ti electrode with Si substrate. (d)–(f) *P–V*/*I–V* measurements for W, Pt/Ti/TiN, and Pt/Ti electrodes at a smaller voltage sweep range.

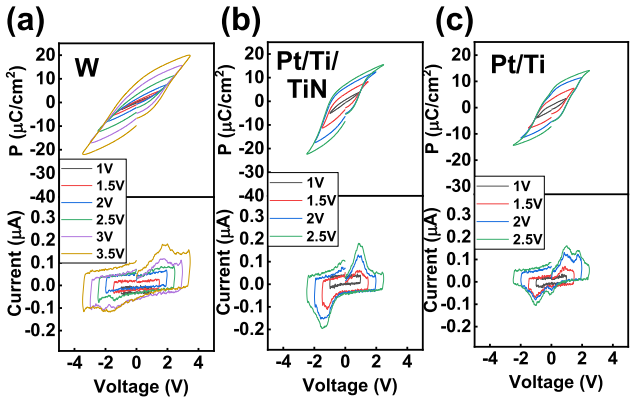

Fig. 4. *P–V* and *I–V* measurements for three electrode structures on FE MIM capacitors. (a) W electrode with FE MIM structure at various voltage sweep ranges. (b) Pt/Ti/TiN electrode with FE MIM structure. (c) Pt/Ti electrode with FE MIM structure. Note that all have TiN bottom electrodes.

top electrodes at different voltage sweep ranges. W electrode capacitor shows the greatest V_c and the lowest P_r. Pt/Ti electrode capacitor shows a lower V_c compared to Pt/Ti/TiN electrode capacitor may be due to changes in the FE layer grain structure. This data was used for V_c and P_r comparison to the metal-insulator-semiconductor (MIS) structures.

The coercive voltage and remanent polarization for the Si, Ge, and MIM capacitors are compared in Fig. 5. Si-based capacitors show greater V_c when compared to Ge capacitors consistent with the presence of a thick low-κ IL which drives the V_c higher. Conversely, Ge-based capacitors show a significant reduction in V_c with Pt/Ti top electrode consistent with IL thinning. Since Ti, TiN, and W have very similar work functions (Ti $\sim$ 4.33 eV, TiN $\sim$ 4.65 eV, W $\sim$ 4.5 eV), such a large change (1.5 V drop in V_c) cannot be explained

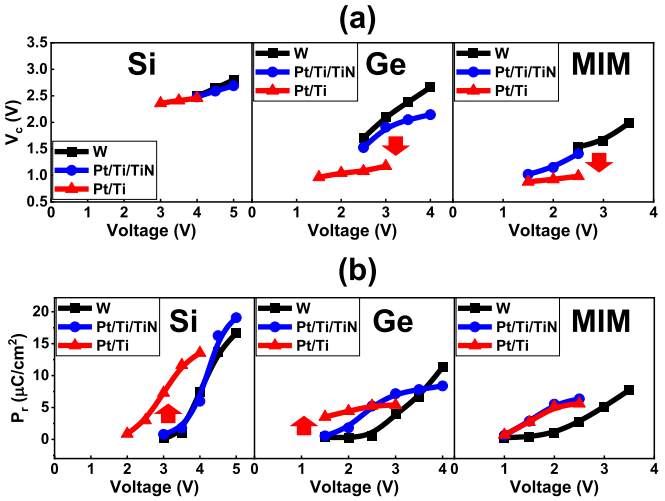

Fig. 5. MOS and MIM Comparison. (a) Variation of V_c with different sweep voltages for MOS and MIM structures with different electrodes (as shown in Figs. 2–4). (b) Variation of P_r with different sweep voltages for MOS and MIM structures with different electrodes (as shown in Figs. 2–4).

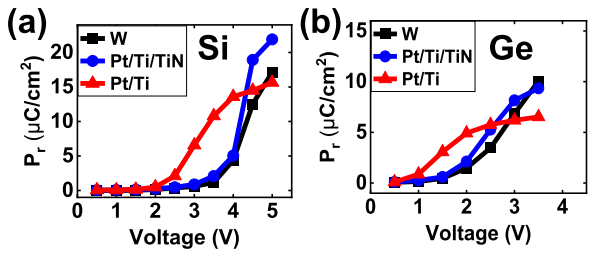

Fig. 6. PUND measurements of Si or Ge MOS structures with different electrodes. (a) Si MOS. (b) Ge MOS.

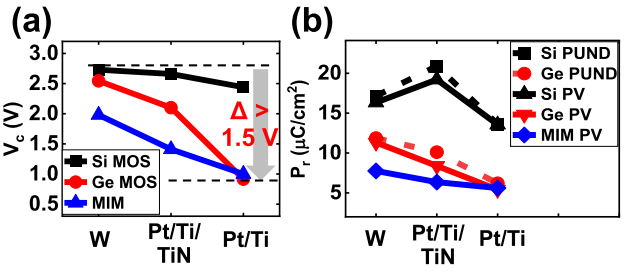

Fig. 7. (a) Comparison of V_c in MOS and MIM structures with different electrodes. (b) Comparison of P_r in MOS and MIM structures with different electrodes.

by metal work function. In both MOS capacitors, the highest V_c is observed with W electrodes since WO_x formation is not favored over SiO_2 and GeO_x resulting in no IL thinning. The data is consistent with a greater fraction of the applied voltage being observed by the FE layer as the IL thickness is reduced, resulting in more FE switching. This effect can be observed in the P_r enhancement shown in Fig. 5(b) at lower voltages for all three sets of capacitors.

Fig. 6 shows P_r as a function of the voltage sweep range extracted from the PUND measurement for Si MOS and Ge MOS. For the PUND measurement setup, the triangle pulse scheme with a frequency of 1 kHz is used. The rising and falling times for the pulses are both 250 μs. From the PUND

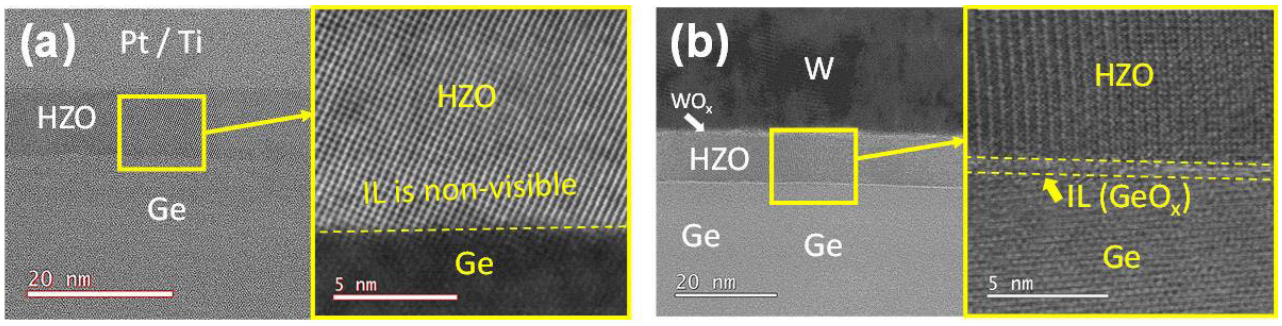

Fig. 8. Cross Section HR-TEM images of MIS stacks on Ge. (a) "Pt/Ti" electrode (oxygen-scavenged). (b) "W" electrode (W, non-scavenged). Although the "W" electrode shows an IL, Pt/Ti' electrode does not show any IL since oxygen in GeO_x reacted with Ti and formed TiO_2.

measurement results, it is evident that the Si and Ge MOS capacitors with Pt/Ti electrodes exhibit the lowest V_c which is consistent with the previous results shown in Figs. 2(d)–(f) and 3(d)–(f).

The maximum values of V_c and P_r are plotted as a function of the top electrode structure for FE MOS capacitors on Si and Ge and FE MIM capacitors in Fig. 7(a) and (b), respectively. In Fig. 7(a), the V_c is defined as half of the difference between V_c and V_{c-} [$V_c = 1/2(V_{c+} - V_{c-})$], where V_{c+} and V_{c-} are obtained from the voltage at which the switching current reaches its maximum value in the I–V loop. For comparison, the P_r values extracted from the PUND measurements are also plotted as a function of the top electrode structure for the FE MOS capacitor on Si and Ge and are shown in Fig. 7(b).

As shown in Fig. 7(a), V_c decreases for FE MIM capacitors as the electrode is changed from W to Pt/Ti/TiN to Pt/Ti. This indicates that the top electrode changes the properties of the FE layer. Unlike MOS capacitors with interlayers such as GeO_x and SiO_x, there is no oxygen scavenging in MIM capacitors. However, oxygen from the HZO layer can mitigate to Ti layer, potentially forming TiO_2. As a result, MIM capacitors can exhibit the P–V dependence of top electrode metals, and devices with the "Pt/Ti" top electrode can demonstrate reduced polarization. However, the V_c change in MIS cannot be explained by the change in the FE layer since the Si channel shows only a small reduction in V_c when compared to the Ge channel MIS capacitor. The reduction of V_c in the FE MOS capacitor on Ge is much greater than that for V_c in the FE MIM capacitors (1.6 versus 0.9 V) confirming that IL scavenging is effective in reducing V_c on Ge. In Fig. 7(b), PUND and P–V measurements are largely consistent on Si and Ge substrates. They show the same trend in all three electrodes. It is worth noting that the impact of the substrate on P_r in the FE MOS capacitor is more significant than that of the top electrode.

To investigate the IL thickness reduction, cross-sectional high-resolution transmission electron microscope (HR-TEM) analysis was carried out as shown in Fig. 8. A visible IL is seen in the FE MOS capacitors with a W top electrode on Ge [Fig. 8(a)] while an IL is not visible in the Ge capacitor with a Pt/Ti top electrode [Fig. 8(b)].

In the FE MOS capacitor on Ge with a W electrode [Fig. 8(b)], an IL between HZO and W layers is observed. It can potentially be WO_x. However, since the V_c of the Pt/Ti sample is much less than both W and Pt/Ti/TiN samples, the effect on the V_c of WO_x is not significant. Furthermore, it is expected that the IL thickness in the FE MOS capacitor on Ge with Pt/Ti/TiN will be in between those for W and Pt/Ti electrodes. However, based on the capacitance values, the difference in IL thickness between the FE MOS capacitors on Ge with Pt/Ti/TiN and Pt/Ti is expected to be less than 0.2–0.3 nm which is not detectable by the STEM technique. As such, the STEM image for the FE MOS capacitors on Ge with Pt/Ti/TiN is not shown.

The reduction of V_c in the FE MOS capacitor on Si is smaller than that for V_c in the FE MIM capacitors (0.3 versus 0.9 V). This suggests that even though the top electrode reduces the V_c of the FE layer, it does not greatly reduce the thickness of the SiO_2 IL in the FE MOS capacitor on Si and the voltage drop across the SiO_2 IL dominates the overall V_c of this device. Since the reduction in the thickness of the SiO_2 IL is not as significant as that of the Ge IL, only TEM data on Ge was presented in this article. However, a recent study has reported TEM data on Si with a Pt/Ti/TiN electrode [16].

The C–V characteristics of MOS capacitors are shown in Fig. 9(a) and (b). Fig. 9(c) shows a clear trend in accumulation capacitance enhancement for Ge capacitors when the reactive top electrode is used consistent with thinning of low-κ IL which results in a lower effective oxide thickness (EOT). Conversely, the capacitance for the FE MOS capacitor on Si is nominally independent of the top electrode. The capacitance of FE MOS capacitors on Ge varies significantly with the change of the electrode from 2.6 to 0.9 μF/cm^2 as the electrode is changed from Pt/Ti to W, a total of 2.6–0.9 = 1.7 μF/cm^2 change. Conversely, the change of the capacitance of the FE MOS capacitors on Si with the choice of an electrode is much smaller compared to that in FE MOS capacitors on Ge from 0.3 μF/cm^2 on Si to 1.7 μF/cm^2 on Ge. This is consistent with less IL scavenging in Si compared to Ge. The impact of the Pt/Ti electrode is greater than Pt/Ti/TiN since Ti in direct contact with the gate oxide is more reactive than when Ti is stacked on even thin TiN [15], [16]. The results show that the oxygen-scavenging by Ti is more effective on Ge substrates than on Si substrates consistent with the lower thermodynamic stability of the GeO_x native oxide. The enthalpy of formation for SiO_2, GeO_2, and TiO_2 are −911, −580, and −939 kJ/mol, respectively [19], [20]. The enthalpy difference between GeO_2 and TiO_2 (∼359 kJ/mol) is ten times larger than the difference between SiO_2 and TiO_2 (∼28 kJ/mol). The thermodynamics

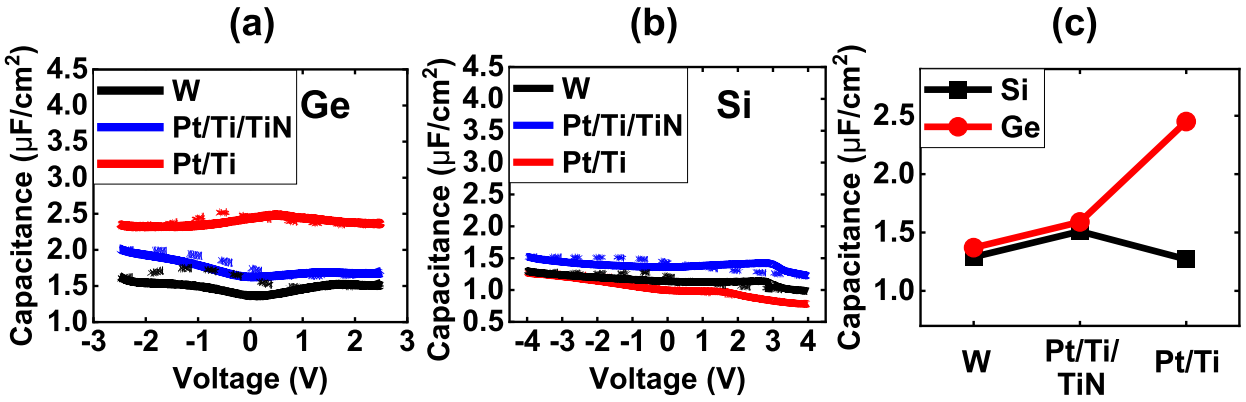

Fig. 9. MIS Capacitances with Different Electrodes. (a) *C–V* characteristics of the HZO-based MOS capacitors on Ge with the three different top electrodes. (b) *C–V* characteristics on Si with varied top electrode conditions. (c) Comparison of capacitance for Si and Ge samples with different electrodes.

are consistent with the presence of a highly reactive Ti layer in the top electrode readily extracting oxygen from the unstable GeO_x layer and thereby scavenging the IL resulting in an IL-free interface between HZO and Ge. The intermediate TiN layer between Ti and FE-IL structure acts as a barrier for Ti diffusion into HZO. However, the reduction in V_c is less than Pt/Ti electrode but an improvement over the W electrode can still be observed.

IV. Conclusion

Oxygen scavenging was demonstrated to be an effective way to reduce the V_c of FE HZO-based MOS structures on Ge semiconductors. The V_c as low as 0.9 V was observed in 10 nm FE HZO gate stacks on Ge with Pt/Ti electrodes. The oxygen-scavenging technique is found to be more effective on Ge substrate yielding a 66% (>1.5 V) reduction in V_c as compared to 9% (<0.5 V) in Si. The reduced V_c demonstrated in this work by adopting Ge, and the scavenging scheme will give helpful insight for future research on FEFETs.

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